Paper No. 11

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHWAN-YING LEE and TZUEN-HSI HUANG

Appeal No. 1999-2739
Application No. 08/891,127

ON BRIEF

Before KIMLIN, WALTZ, and TIMM, Administrative Patent Judges.
WALTZ, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1 through 10, 12 through 14, 16 through 21, and 25 through 28, which are the only claims remaining in this application.[1]

According to appellants, the invention is directed to a submicron interconnection using a nickel electroless process on

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[1] Appellants' amendment subsequent to the final rejection has been entered (see the Amendment dated Oct. 16, 1998, Paper No. 6, and the Advisory Action dated Oct. 28, 1998, Paper No. 7).

polysilicon with a rapid thermal annealing process (Brief, page 3). A copy of illustrative independent claim 1 is attached as an Appendix to this decision.

The examiner has relied upon the following references as evidence of obviousness:

Patel et al. (Patel)	4,321,283	Mar. 23, 1982
Takeuchi	5,097,300	Mar. 17, 1992
Lee et al. (Lee) (filed Jan. 2, 1996)	5,658,815	Aug. 19, 1997

Claims 1, 3-10, 12, 13, 16-21, 25, 27 and 28 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Takeuchi in view of Patel (Answer, page 3). Claims 2, 14, and 26 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Takeuchi in view of Patel and Lee (Answer, page 5).[2] We *reverse* all of the rejections on appeal for reasons which follow.

OPINION

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[2] The examiner has not repeated the final rejection of claims 2, 14 and 26 under the second paragraph of 35 U.S.C. § 112 (see the Final rejection, Paper No. 5; the Advisory Action, Paper No. 7; and the Brief, pages 5-6). This rejection has not been specifically withdrawn (see the Answer). However, rejections that are not repeated in the Answer are considered as withdrawn. *See Paperless Accounting v. Bay Area Rapid Transit Sys.*, 804 F.2d 659, 663, 231 USPQ 649, 652 (Fed. Cir. 1986).

The examiner finds that Takeuchi teaches a semiconductor device where a semiconductor substrate (101) is coated with an oxide film (102), followed by deposition of a polysilicon film (103) to a thickness of 1000 to 3000 •, in turn followed by deposition of a refractory metal film or molybdenum film (104) by sputtering (Answer, page 3). The examiner further finds that unnecessary portions of the films are removed by photoetching to form a gate electrode, followed by thermal annealing at a temperature of 850 to 1100•C. with the result that the molybdenum film (104) reacts with the polysilicon film (103) thereby creating a molybdenum silicide layer (105)(*id.*). The examiner also finds that Takeuchi teaches that the refractory metal film (104) can be formed by metals such as nickel (*id.*).

The examiner recognizes that Takeuchi fails to teach the rapid thermal annealing as required by part c) of claim 1 on appeal (*id.*, last sentence). However, the examiner's position is "that one skilled in the art ... would have had a reasonable expectation of achieving similar success" regardless of whether the metal layer was thermally annealed as in Takeuchi or underwent rapid thermal annealing as required by the claims,

citing as support the fact that the metal layer in both instances is heat treated to form a metal silicide layer (Answer, page 4). We disagree.

We determine that the examiner has no basis in evidence or convincing reasoning to support his position and legal conclusion. The examiner has not pointed to any evidence or convincing reasons why one of ordinary skill in the art would have had a reasonable expectation of achieving success by *lowering* the annealing temperatures of Takeuchi to those recited in claim 1, much less why one of ordinary skill in the art would have limited the anneal to 30-60 seconds in a nitrogen atmosphere when the examiner has not shown that these conditions were even recognized by Takeuchi. *See In re Zurko,* 258 F.3d 1379, 1385, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001)(The deficiencies of a reference cannot be remedied by the PTO's general conclusions of "basic knowledge" or "common sense").

The examiner also finds that Takeuchi fails to teach depositing the nickel by electroless deposition instead of sputtering (Answer, page 4). To remedy this deficiency, the

examiner applies Patel for the teaching of electroless nickel plating onto a silicon substrate (*id.*).

Appellants argue that Patel is directed to electroless deposition of nickel onto a silicon substrate, not the *polysilicon* substrate required by claim 1 on appeal (Brief, pages 8 and 15). Appellants also argue that there is no motivation to combine Patel and Takeuchi (Brief, page 7). We agree.

The examiner has failed to establish why one of ordinary skill in this art would have taken the electroless nickel deposition onto silicon, as taught by Patel, and used this method on the polysilicon substrate of Takeuchi. Furthermore, the examiner has not even attempted to present any teaching, suggestion, or motivation to combine these references as proposed in the examiner's rejection (Answer, pages 4-5). *See In re Dembiczak,*

175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)(The showing or evidence of a suggestion, teaching, or motivation

to combine must be clear and particular). The examiner has not identified, on this record, any teaching or motivation (e.g., advantages) for using electroless nickel deposition instead of the sputtering taught by Takeuchi.[3]

The examiner has applied Lee in addition to Patel and Takeuchi in the rejection of claims 2, 14 and 26 (Answer, page 5). However, Lee has been cited for the teaching of wet etching the remaining nickel from the silicon substrate (*id.*) and therefore does not remedy the deficiencies discussed above.

For the foregoing reasons, we find that the examiner has failed to establish a *prima facie* case of obviousness in view of the reference evidence. Accordingly, we need not review appellants' rebuttal evidence of unexpected results (Brief, page 12). *See In re Geiger,* 815 F.2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987). Therefore the rejections under 35 U.S.C.

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[3] We note that Patel teaches a method of nickel deposition which renders unnecessary any catalyzing pretreatment of the silicon surface that is to receive the nickel (abstract). However, we find that Takeuchi deposits nickel onto polysilicon and does not teach any catalyzing pretreatment of this surface.

§ 103(a) over Takeuchi in view of Patel and Takeuchi in view of Patel and Lee are reversed.

The decision of the examiner is reversed.

REVERSED

EDWARD C. KIMLIN Administrative Patent Judge	)
THOMAS A. WALTZ Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
CATHERINE TIMM Administrative Patent Judge	)

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APPENDIX

1. A method for a Nickel silicide formation in an integrated circuit by Electroless Ni deposition on Polysilicon and rapid thermal annealing comprising the following steps:

a) forming and patterning a polysilicon layer over a substrate;

b) selectively electroless depositing Nickel over said polysilicon layer forming a Nickel layer over said polysilicon layer;

c) rapidly thermally annealing said substrate forming a nickel silicide layer over said polysilicon layer; said nickel silicide layer forming part of a semiconductor integrated circuit device;
said rapid thermal anneal is performed at a temperature in a range of between about 400 and 750°C for a time in a range of between about 30 and 60 sec and with a nitrogen flow whereby said nickel silicide layer does not have agglomeration.

Jenine Gillis

JUDGE WALTZ

APPEAL NO. 1999-2739

APPLICATION NO. 08/891,127

APJ WALTZ

APJ TIMM

APJ KIMLIN

DECISION: **REVERSED**

PREPARED: Jul 25, 2002

OB/HD

PALM

ACTS 2

DISK (FOIA)

REPORT

BOOK

GAU: 1700

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KENNETH D. CHAPMAN
and
STEVEN P. YOUNG

Appeal No. 2000-1204
Application No. 08/786,818

HEARD: FEBRUARY 21, 2002

Before HAIRSTON, RUGGIERO, and SAADAT, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 3, 4 and 7 through 10.

The disclosed invention relates to the use of a dedicated AND gate in a configurable logic block (CLB). The CLB is used in a field programmable gate array.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

> 1. A configurable logic block (CLB) for use in a field programmable gate array, the CLB comprising:
>
> a plurality of input lines;
>
> a carry-in line;
>
> a carry-out line;
>
> at least one lookup table, each such lookup table receiving input signals from N of the plurality of input lines and having an output line;
>
> a dedicated AND gate receiving two input signals from two of the plurality of input lines; and
>
> a carry chain having a carry input coupled to the carry-in line and a carry output coupled to the carry-out line, and at least one carry multiplexer controlled by the lookup table output line, each such multiplexer having at least two inputs, one such input being provided by the carry-in line, and the other such input being provided by the AND gate.

The references relied on by the examiner are:

New et al. (New) 5,481,206 Jan. 2, 1996
Rose et al. (Rose) 5,724,276 Mar. 3, 1998
(filed Jun. 17, 1996)

Claims 1 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rose.

Claims 4 and 7 through 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rose in view of New.

Reference is made to the briefs (paper numbers 15 and 17) and the answer (paper number 16) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1, 3, 4 and 7 through 10.

The examiner's rejection is as follows:

> As per claim 1, Rose et al[.] discloses in Fig. 4a a configurable logic block (CLB) for use in a field programmable gate array (FPGA). The CLB clearly has a plurality of input lines, a carry-in line, a carry-out line, at least one lookup table (LUT F), and a carry chain having a carry input coupled to the carry-in line and a carry output coupled to the carry-out line. The carry chain also has at least one carry multiplexer (CMUX) controlled by the output of the lookup table and having one input being provided with the carry- in line and another input being provided with an AND logic of 2 input lines (a0b1) which are also the input lines to the lookup table. It [is] noted that Rose et al. discloses the AND logic being provided by another lookup table (LUT G), whereas, in the present invention the AND logic [is] being provided by a dedicated AND gate. However, in the field of FPGA, the use of a lookup table and the use of a gate to provide a logic function are both well known and are art recognized equivalents with a trade off between

the complexity and the flexibility of a CLB. Further, since Rose et al. clearly disclose in Fig. 4a that an output of the CMUX is provided with an AND logic of 2 input lines (a0b1) of the LUT F, a person of ordinary skill in the art

> would have found it obvious to provide Rose et al. with an AND gate in place of the LUT G for providing the AND logic to the CMUX in order to reduce the circuitry in the CLB. [Answer, pages 3-4.]

Appellants argue inter alia (brief, pages 4 and 5) that "the Office Action has not provided any support for its assertion that 'the use of a LUT and the use of a logical gate for providing a logical function are art recognized equivalents,'" and that "it is insufficient to assert that one of ordinary skill in the art might have been motivated to replace LUT G with a random single gate."

In In re Zurko, 258 F.3d, 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001), the Court stated that:

> With respect to core factual findings in a determination of patentability . . . the . . . [Office] cannot simply reach conclusions based on its own understanding or experience - or on its assessment of what would be basic knowledge or common sense. Rather, the . . . [Office] must point to some concrete evidence in the record in support of these findings.

In view of the complete absence of any evidence in the record to support the examiner's finding that "the use of a lookup table and the use of a gate to provide a logic function are both well known and are art recognized equivalents," we cannot agree with the examiner that the skilled artisan would have

found it obvious "to provide Rose et al. with an AND gate in place of the LUT G for providing the AND logic to the CMUX." To the contrary, it appears that the LUT G performs an arithmetic multiplication function, as opposed to a logical ANDing function, when it "performs the calculation a**0**b**1**" (column 3, lines 23 and 24; Figure 4a). In the absence of such evidence, the examiner has not presented a prima facie case of obviousness of the claimed subject matter. Thus, the obviousness rejection of claims
1 and 3 is reversed. The obviousness rejection of claims 4 and
7 through 10 is likewise reversed because the multiplexer teachings of New do not cure the noted shortcomings in the teachings of Rose and the examiner's finding of obviousness.

DECISION

The decision of the examiner rejecting claims 1, 3, 4 and 7 through 10 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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) BOARD OF PATENT
JOSEPH F. RUGGIERO) APPEALS AND
Administrative Patent Judge) INTERFERENCES
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KWH:hh

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